		Bit3	Bit2	Bit1	Bit0		Motor#2	Motor#1
		SSR#4	SSR#3	SSR#2	SSR#1		Digital Pot#2	Digital Pot#1
Action	Hex Data	**Right Rev**	**Right Fwd**	**Left Rev**	**Left Fwd**	**Hex Data**	**Right Speed**	**Left Speed**
Stop	**0**	0	0	0	0	**0**	don't care	don't care
Fwd Pivot Right	**1**	0	0	0	1	**1**	don't care	>0
Rev Pivot Right	**2**	0	0	1	0	**2**	don't care	>0
Fwd Pivot Left	**4**	0	1	0	0	**4**	>0	don't care
Forward	**5**	0	1	0	1	**5**	>0 &=Left	>0 &=Right
Fwd Veer Right	**5**	0	1	0	1	**5**	>0	>Right
Spin CCW	**6**	0	1	1	0	**6**	>0 &=Left	>0 &=Right
Rev Pivot Left	**8**	1	0	0	0	**8**	>0	don't care
Spin CW	**9**	1	0	0	1	**9**	>0 &=Left	>0 &=Right
Reverse	**A**	1	0	1	0	**A**	>0 &=Left	>0 &=Right
Rev Veer Left	**A**	1	0	1	0	**A**	>Left	>0

		Wire	**S/C Term**	**Pot**	
Speed Control		**RED**	VREF	VH	5V
Pot Hookup		**YEL**	DC IN	VW	
		BLU	GND	VL	GND

Control Hookup		**GND**	**U/D**	**INC**	**CS**	**VCC**
L Speed Control	**MEGA**	-				-
R Speed Control	**MEGA**	-				-

Motor Control Relays Wired to Center PCB Card Drive Through Digital Logic Circuits

	Color	PCB Term	Color	PCB Term		PCB Term	MEGA Outputs
5VDC	Copper	1					
Left FWD (LF)	**GRN**	5	**BLK**	6			
Left REV (LR)	**BLU**	3	**RED**	4			
Right FWD (RF)	**GRN**	10	**BLK**	11			
Right REV (RR)	**BLU**	8	**RED**	9			
GND	Copper	22					

Bumper Sensors Wired to Center PCB Card PCB has 44 contact (1 to 22) and (A to V)

		PCB Term		MEGA Inputs	MEGA Output	MEGA Latched Sensor Inputs
Left Front Bumper	**GRN**	14	Ground to activate			
Center Front Bumper	**RED**	15	Ground to activate			
Right Front Bumper	**BRN**	13	Ground to activate			
Rear Bumper	**BLK**	16	Ground to activate			
LATCH RESET			Ground to activate			
GND	Copper	22				

The bumper switches will be wired through latching logic that disables the respective motor control relays (i.e. The front bumpers will turn off either forward motor relay. The rear bumper will turn off either reverse motor relay.) The LATCH RESET will only be used if no sensor switch is activated.

	IN1	IN2	OUT
Two-Input AND Gate	0	0	0
	0	1	0
	1	0	0
	1	1	1

	IN1	IN2	OUT
Two-Input OR Gate	0	0	0
	0	1	1
	1	0	1
	1	1	1

	IN1	IN2	OUT
Two-Input NAND Gate	0	0	1
	0	1	1
	1	0	1
	1	1	0

	IN1	IN2	OUT
Two-Input NOR Gate	0	0	1
	0	1	0
	1	0	0
	1	1	0

	IN1	IN2	OUT
Two-Input XOR Gate	0	0	0
	0	1	1
	1	0	1
	1	1	0